Test architecture and method

The present invention relates to a test access architecture and method for testing an electronic circuit, and in particular to a test access architecture and method for modular testing a system on chip (SOC).

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Modern semiconductor design methods and manufacturing technologies enable the creation of a complete system on one single die, the so-called "system chip" or SOC. Such system chips are typically very large integrated circuits, consisting of millions of transistors, and containing a variety of hardware modules. In order to design these large and
10   complex system chips in a timely manner and leverage from external design expertise, reusable cores are increasingly being used. Cores are pre-designed and pre-verified design modules that are intended for re-use in multiple SOC designs. Examples of cores are CPUs, DSPs, media co-processors, communication modules, memories, and mixed-signal modules.

Due to imperfections in their manufacturing process, all integrated circuits
15   need to be individually tested for manufacturing defects. System chips are no exception to that rule. Modular test development is increasingly used for SOCs. Non-logic modules, such as embedded analog circuitry and memories require stand-alone testing due to their "abnormal" circuit structure. Black-boxed third-party cores, such as hard (layout) cores and encrypted cores, for which no implementation details are known, need to be tested by the
20   tests supplied by their provider, and therefore also require stand-alone testing. Furthermore, even for logic modules of which the implementation details are known, modular test development is an attractive alternative. Here, a modular "divide-and-conquer" test development approach helps to reduce the test generation compute time and associated data volume. Finally, a modular test approach enable test reuse, which is especially beneficial if a
25   core or module is used in multiple SOC designs.

In order to enable modular test development, an embedded module should be isolated from its surrounding circuitry and electrical test access needs to be provided. A paper by Zorian et al, Proceedings of the IEEE International Test Conference (ITC), pages 130-143, Washington DC, October 1998, describes a generic conceptual test access architecture

enabling modular testing of SOCs. The test access architecture consists of three main elements per module under test. These comprise (1) a test pattern source and sink, (2) a test access mechanism (TAM), and (3) a wrapper. The wrapper can isolate the module from its surroundings and provides switching functionality between functional access to the module

5   and test access through the TAM. A SOC test access architecture determines the number of distinct TAMs and their widths, the assignment of modules to TAMs, and the design of the test wrappers.

The design of a test access architecture is typically constrained by the total amount of TAM wires "w" and the number of modules "m" to be tested. The number of TAM

10   wires w is dictated, for example, by the number of available IC pins, the amount of TAM wiring area the SOC designer wishes to spend, or by other practical constraints. Given w and the number of modules m to be tested, the SOC designer has to determine the number of separate TAMs and their individual widths w_i (such that $\sum w_i \leq w$) and the assignment of modules to TAMs (such that every module is connected to exactly one TAM).

15   One possibility is to create a separate TAM for each module. This only works if the number of modules m is less than or equal to the number of TAM wires w. This type of test access architecture is referred to as a "Distribution" architecture. The challenge of designing a Distribution architecture is to optimize the individual TAM widths w_i such that the overall test time is minimized. Another possibility is to create one single TAM of width

20   w, to which all modules are connected. Such a test access architecture is referred to as a "Daisychain" architecture.

The Distribution and Daisychain architectures form two extremes of an entire spectrum of architectures, which are referred to as "Hybrid TAM Architectures". These architectures consist of a number of separate TAMs, while every TAM services the test

25   access needs of a number of modules.

Figure 1 shows a typical hybrid TAM Architecture for a SOC. The SOC contains twenty eight modules 3 that need to be tested individually (ie $m = 28$). This test access architecture 1 consists of nine distinct TAMs 5_1 to 5_9. In the example, the TAMs 5_1 to 5_9 have the following respective widths: 23, 6, 4, 3, 5, 10, 6, 6, 1. This gives a total TAM

30   width w of 64 wires. The module assignment vector for this architecture is (5_6; 5_8; 5_4; 5_3; 5_2; 5_6; 5_4; 5_7; 5_3; 5_9; 5_6; 5_5; 5_9; 5_9; 5_9; 5_9; 5_3; 5_2; 5_3; 5_3; 5_7; 5_9; 5_9; 5_9; 5_5; 5_1; 5_9; 5_9). In other words, the first of the modules 3 is assigned to TAM 5_6, the second module to TAM 5_8, the third module TAM 5_4, and so on for the twenty eight modules.

Figure 1 therefore shows the widths of the individual TAMs 5_1 to 5_9, and the assignment of the various modules 3 to the TAMs 5_1 to 5_9. The design of the test access architecture has a large impact both on the required vector memory depth per tester channel, as well as on the test application time of the SOC, two key parameters in the overall SOC test

5   cost.

While the two extremes of the spectrum, i.e., Distribution and Daisychain architectures have proved popular with SOC design teams that do not have access to automated test access architecture design tools, research has shown that in virtually all cases, these two architectures result is significantly longer test times than the Hybrid TAM

10   Architectures.

From the above, it can be concluded that, in many situations, in order to minimize the required tester vector memory and test application time, it is desirable to design a test access architecture in which multiple modules are connected to a common TAM, for example as shown in TAMs 5_2, 5_3, 5_4, 5_5, 5_6, 5_7, and 5_9.

15   When multiple modules 3 are connected to a common TAM 5 in this manner, it must be ensured that the test data of each module 3 in that TAM 5 can reach the SOC pins. Therefore, each module 3 needs to have a "transparent mode", in which test pattern data of another module can be transported along this module. It is noted that transporting the test pattern data involves the transportation of test stimulus data to the module being tested, and

20   the transportation of test response data from the module being tested. Two known examples for providing this "transparent mode" are shown in Figures 2A and 2B. The transparent test access path in both figures is indicated by means of the bold lines.

In Figure 2A, a test access method hereinafter referred to as "through module" is illustrated. The module 3 is shown with a test wrapper 7, which receives a number of test

25   signals, including a global scan enable signal 27 (se). The global scan enable signal 27 is provided for placing the module in scan test mode. According to this arrangement, TAM inputs 21 and TAM outputs 23 form connected scan chains, with wrapper input cells, module internal scan chains 25, and wrapper output cells as their elements. This makes it possible to scan through all these elements. The benefit of this approach is that it does not require

30   additional hardware, since it simply makes use of the existing wrapper and scan chain infrastructure. The drawback of this approach is that the resulting test times depend on the length of these wrapper scan chains, and hence can be extremely long. In other words, test stimulus data must be shifted into a module under test (possibly though a number of other modules), and then the test response data shifted out to the SOC pins (again possibly through

a number of other modules). It will be appreciated that the test response data from one test must be shifted out before the next test stimulus data can be launched and the corresponding test response data captured, otherwise the test response data from the first test will be corrupted by another module.

5   In Figure 2B, a test access method hereinafter referred to as "via bypass" is illustrated. As before, the test wrapper 7 receives a plurality of test signals, including a global scan enable signal 27 (se). According to this arrangement, the test access method makes use of dedicated hardware comprising bypass wires 28 and bypass logic 29. At the expense of this additional on-chip hardware, ie necessary for the implementation of the

10   bypass, the time required for transporting test pattern data of other modules along this module is substantially reduced. In other words, when transporting test stimulus data to a particular module under test, the test stimulus data bypass all modules located prior to the module under test, while the test response data from the tested module bypass all modules located after the module under test.

15   The operation of the arrangements described above will now be explained in relation to Figures 3A and 3B, which illustrate schematically how two modules are connected according to the test access architectures of Figures 2A and 2B, respectively. It will be appreciated that only two modules have been shown for simplicity, but that the invention is equally applicable to any number of modules being connected in this manner.

20   In Figure 3A, module A is connected to module B in the "through module" format. Module A comprises internal scan chains 31 and 33 which receive test stimulus data from the input TAM wires 35. The output 37 of the scan chains 31 and 33 of module A form the input 38 of internal scan chains 39 and 41 of module B. The output 43 of scan chains 39 and 41 are in turn passed to a further module, or to the SOC pins (not shown). A common

25   scan enable signal 27 (se) is connected to each of the modules A and B. Therefore, in operation, when testing module A, test stimulus data is shifted into module A, and the scan enable signal 27 activated. This results in both modules A and B entering the scan test mode together, whereby the test stimulus data in module A is launched, and the test response data captured. Once the test stimulus data has been launched and the test response data captured,

30   the scan enable signal 27 is deactivated, and the test response data from module A must then be shifted out through module B. However, so that the test response data is not corrupted on its path to the output, the scan enable signal 27 cannot be activated again until the test response data has been shifted through module B, otherwise the test response data will be corrupted by module B. This results in the test time being increased, since the next test

stimulus data for module A cannot be launched (and the test response data captured) until the test response data from the previous test has been shifted out past module B. In a similar manner to the above, to test module B the test stimulus data for module B needs to be shifted though module A, which also results in an increased test time. The above problems are

5   increased further when more than two modules are connected in series on the same TAM.

In contrast, Figure 3B shows how two modules A and B are connected in the "bypass" mode. According to this arrangement, the architecture comprises additional bypass hardware comprising multiplexers 47 and 49, and additional bypass wires 51 and 53. In effect, the input wires 35 to module A are also connected to the multiplexer 47. This means

10   that when module B is being tested, the test stimulus data from input wires 35 is passed directly to the input of module B via the wires 51 and multiplexer 47, thereby bypassing module A. Likewise, when module A is being tested, the test response data output on wires 37 from module A can be transported via the multiplexer 47, the bypass wires 53 and multiplexer 49, thereby bypassing module B.

15   It is noted that, in this arrangement, both modules A and B receive the common scan enable signal 27. However, a dedicated bypass signal 55 is provided for bypassing module A, while a dedicated bypass signal 57 is provided for bypassing module B.

Basically, the two alternatives described above provide a trade-off between (1) low silicon area at the expense of large test time, versus (2) short test time at the expense of

20   additional silicon area. In order to appreciate the benefits and costs of each option, the tradeoff for a typical SOC design having 57 different modules and a total test rail width of 142 wires will be discussed. Implementing bypasses for all wires and all modules would cost 57 x 142 = 8094 additional multiplexers and flip flops. In terms of additional flip flops, this adds 3% to the overall flip flop count. From this, it can be concluded that the silicon area

25   costs of adding bypasses to all modules are substantial. On the other hand, not implementing bypasses makes the overall test data volume increase by 12% from 1.52 Mbit/pin to 1.73 Mbit/pin. Hence, the additional test time costs of not implementing bypasses are substantial as well.

In the light of the above, the aim of the present invention is to provide a test

30   access architecture and method that allows the shorter test times of the bypass implementation to be achieved, but at substantially lower silicon area costs.

According to the present invention, there is provided a test access architecture for testing modules in an electronic circuit, the test access architecture comprising:

- a test access mechanism (TAM) having a plurality of modules connected in series thereto, the test access mechanism arranged to transport test stimulus data to, and test response data from a module being tested;

- a global enable signal, the global enable signal provided for placing the modules in a test mode; and

- a control circuit provided between the global enable signal and an associated module, wherein the control circuit is arranged to control whether or not the global enable signal is passed to its associated module.

The invention has the advantage of enabling the test time to be reduced, but without increasing the silicon area to the extent required by the bypass method.

Preferably, the control circuit is controlled by a dedicated bypass signal for that particular module.

The control circuit is connected to receive the global enable signal and the dedicated bypass signal, and arranged to provide a local enable signal to its associated module based on the respective states of the global enable signal and the dedicated bypass signal.

This has the advantage of allowing the control circuit to pass the global enable signal if its associated module is being tested, and to block the global enable signal if its associated module is not being tested.

Preferably, the control circuit is an OR gate. Alternatively, depending on the control signals being used, the control circuit may be another logic gate, such as an AND gate.

The control circuit is preferably located within a test wrapper of its associated module. Alternatively, the control circuit may be located in a test control block of a system on chip (SOC), or within the module itself.

Preferably, the test stimulus data and test response data is processed in a pipelined manner, thereby enabling the test time to be reduced further.

According to another aspect of the invention, there is provided a method of testing a module in an electronic circuit, the module being one of a plurality of modules connected in series to a test access mechanism (TAM), the test access mechanism arranged to transport test stimulus data to a module being tested, and to transport test response data from the module being tested, the method comprising the steps of:

-           loading a first set of test stimulus data into the module being tested;

-           testing the module in response to a global enable signal being activated;

-           unloading test response data captured from the module being tested;

wherein, during the testing step, other modules connected to the test access mechanism

5   (TAM) are placed in a transport mode of operation, such that the other modules do not

corrupt a second set of test stimulus data being loaded into, or previous test response data

being unloaded from, the module under test.

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10   For a better understanding of the present invention, and to show more clearly

how it may be carried into effect, reference will now be made, by way of example, to the

accompanying drawings, in which:-

            Figure 1 illustrates a typical test access architecture according to the prior art;

            Figure 2A illustrates a test wrapper for use in the architecture of Figure 1,

15   using a "through module" arrangement;

            Figure 2B illustrates a test wrapper for use in the architecture of Figure 1,

using a "via bypass" arrangement;

            Figure 3A illustrates schematically how two modules are connected according

to the arrangement of Figure 2A;

20   Figure 3B illustrates schematically how two modules are connected according

to the arrangement of Figure 2B;

            Figure 4 illustrates a test access architecture according to a preferred

embodiment of the present invention;

            Figure 5 illustrates a schematic diagram of the test access architecture of

25   Figure 4, in accordance with the present invention;

            Figures 6a to 6h illustrate the method of testing a module using the test access

architecture of Figures 4 and 5.

30   Figure 4 shows a test access architecture according to a preferred embodiment

of the present invention. In a similar manner to the test access architectures of Figures 2A

and 2B, the test access architecture comprises a module 3 having internal scan chains 25, and

connected to receive test stimulus data on TAM input wires 21 and to output test response

data on TAM output wires 23. The module 3 also receives a global scan enable signal 27

(se). It is noted that the global scan enable signal 27 (se) may be a global signal for all modules in the TAM, a group of modules, or even for all modules in the SOC.

According to the invention a control circuit, for example a two input OR gate 59, is provided between the global scan enable signal 27 and the module 3. One input of the OR gate 59 is connected to receive the global scan enable signal 27 (se). The second input of the OR gate 59 is connected to receive a dedicated bypass signal 61. The output of the OR gate 59 provides a local scan enable signal 60, which is connected to wherever the global scan enable 27 (se) used to be connected within the module and its wrapper. Since the dedicated bypass signal 61 is specific to a particular module, this means that each module has a dedicated signal for effectively controlling whether the global scan enable signal 27 is passed to that module. In other words, the dedicated bypass signal 61 acts as a control signal for controlling whether or not the local scan enable signal 60 mirrors the global scan enable signal 27.

Effectively, this implementation enables the global scan enable signal 27 to be kept high for one or more particular modules that are not being tested, by maintaining the dedicated bypass signal 61 high for those particular modules, thereby placing them in a transport mode of operation.

The provision of the logic gate 59 enables the test access architecture to be operated as follows. If, in order to test another module, test stimulus data needs to be transported via this module, the data is transported through this module (as shown in Figures 2A and 3A). However, in order to avoid having additional test time, the transparent modules are allowed to work in a pipelined mode. This means that modules in front of the module-under-test already contain the subsequent test stimulus data to be applied after the current test stimulus data. At the same time, the modules after the module-under-test still contain test response data from previous tests, which are still on their way out to the SOC pins. Since the global scan enable signal 27 will be activated before the previous test response data has been shifted through to the output, the dedicated bypass signal 61 is kept high to prevent the global scan enable signal 27 from reaching the other modules, ie the local scan enable signal 60 remains high in the other modules.

Thus, the neighboring modules, which are not being currently tested themselves, operate in a transport mode of operation, whereby they serve as transport chains to and from the module-under-test, and function as FIFO buffers for either test stimulus data or test response data.

Figure 5 shows a schematic diagram of two modules, modules A and B, connected according to the present invention. Modules A and B each contain two scan chains of lengths eight and six flip flops. For test access, A and B are connected into one common two-bit TAM. Both modules receive a global scan enable signal 27 (se) which, when

5   asserted, makes the corresponding scan chains scan. In accordance with the invention, the global scan enable signal 27 (se) is OR-gated in each module with a dedicated bypass signal 61A, 61B, named bypass_A and bypass_B, respectively.

It is noted that, although the preferred embodiment shows the use of a logic OR gate, it will be readily appreciated by a person skilled in the art that other

10 implementations include those with a logic AND gate (for example, in case of reversed polarities of the global scan enable (se) and bypass signals involved). Furthermore, the gate may be positioned either further away from the local modules (e.g., in a SOC-level Test Control Block (TCB)) or integrated deeper into the local modules (e.g., after a module specific TCB).

15 As described above in Figure 4, a plurality of test stimulus data are shifted into the scan chains of module A, and the corresponding test response data shifted out through module B. However, to avoid increasing the test time, the transparent modules are allowed to work in a pipelined mode. This means that modules in front of the module-under-test already contain the subsequent test stimulus data to be applied after the current test stimulus data. At

20 the same time, the modules after the module-under-test still contain test response data from previous tests, which are still on their way out to the SOC pins. In order to avoid data corruption, each module has a control circuit, for example the OR gates 59A and 59B, for controlling whether or not the global scan enable signal 27 is passed as a local scan enable signal 60A and 60B to the modules 3A and 3B, respectively. For each module that is not

25 being tested (and therefore acting in a "transparent" mode) the associated dedicated bypass signal is kept high, which means that the corresponding local scan enable for that module is kept high, thereby preventing the global scan enable signal 27 from corrupting test pattern data being transported through that module.

Figures 6a to 6h describe the operation of the invention when applying three

30 sets of test stimulus data to Module A. As described above, the scan testing works according the following procedure:

(1)   the first set of test stimulus data is loaded into the scan chains;

(2)   the test stimulus data is launched and the test response data captured into the same scan chains;

(3)   the test response data is off-loaded from the scan chains, while the next set of test stimulus data is loaded into the scan chains, and so on.

At time t=0 as illustrated in Figure 6a, the circuit is shown prior to commencement of testing. The first bit 62 of the TAM contains three 8-bit test stimulus data in a pipelined configuration, each stage of the pipeline being separated by a single clock 65 as will be described later. The second bit 63 of the TAM contains three 6-bit test stimulus data in a pipelined configuration. The second test stimulus data is arranged such that the 8th bit of the 8-bit test stimulus data is adjacent the 6th bit of the 6-bit test stimulus data.

Figure 6b shows the position of the test pattern data after eight clock cycles, ie t=8. It can be seen that the first set of test stimulus data has been loaded into the scan chains of module A. During loading, the global scan enable signal 27 is high. Also, since module A is being tested the dedicated bypass signal 61A for module A is preferably low, while the dedicated bypass signal 61B for module B is preferably high (ie because module B is not being tested).

Figure 6c shows the operation of the circuit at t=9. At this point, the global scan enable signal 27 goes low. Since the dedicated bypass signal 61A is low, the local scan enable signal 60A also goes low, resulting in the first set of test stimulus data being launched into module A, and the corresponding set of test response data being captured in module A. However, since the dedicated bypass signal 61B is high, the local scan enable signal 60B for module B remains high, and therefore no testing is performed in module B.

Figure 6d shows how the second set of test stimulus data is loaded into module A. While this second set of test stimulus data is loaded into module A, it will be noted that the first set of test response data from the previous test is passed into the scan chains of module B, which act as a FIFO buffer. At t=17 the second set of test stimulus data is fully loaded, with the dedicated bypass signal 61A being low, the global scan enable signal 27 high, and the dedicated bypass signal 61B high.

Figure 6e shows the circuit at t=18, in which the global scan enable signal 27 is taken low. Since the dedicated bypass signal 61A is also low, the global scan enable signal 27 causes the local scan enable signal 60B to go low, thus causing the second set of test stimulus data to be launched and the second set of test response data to be captured. Meanwhile, since the dedicated bypass signal 61B is high, the global scan enable signal 27 does not pass to the scan chains of module B, thereby keeping the local scan enable signal 60B for module B high. This means that the first set of test response data previously received from module A is not corrupted in module B.

The global scan enable signal 27 is then taken high, and the third set of test stimulus data loaded into the scan chains of module A, as shown in Figure 6f. As the third set of test stimulus data is loaded, the first and second test response data form the previous tests are shifted out through module B.

5   Figure 6f shows the circuit at t=27, in which the global scan enable signal 27 is taken low. Since the dedicated bypass signal 61A is also low, the global scan enable signal 27 causes the local scan enable signal 60A to go low, thus causing the third set of test stimulus data to be launched and the third set of test response data to be captured in module A . Meanwhile, since the dedicated bypass signal 61B is high, the local scan enable signal

10   60B remains high. This means that the test response data previously received from module A remains unaltered, for shifting out though module B.

Figure 6h shows how the third set of test response data is shifted out though module B.

As depicted in Figures 6a through 6h, the total test time for applying three test

15   patterns to module A takes 35+8 = 43 clock cycles. For a realistic scenario, where the number of scan chains, their lengths, and the pattern counts are one hundred times larger, the calculation becomes as follows: $(800 + 1) \times 300 + 1600 = 241900$ clock cycles.

In comparison, the number of clock cycles required for each of the conventional methods is as follows:

20   1.   Test Access *Through Module* - In this case, the test time for module A is calculated as follows: $800 + 300 \times (1 + 1600) = 481188$ clock cycles. This is an increase of more than 98% compared to what is achieved with the invention. The additional area costs of implementing the invention is limited to one two-input OR gate per module.

2.   Test Access *Via Bypass* - In this case, the test time for module A is calculated

25   as follows: $800 + 300 \times (1 + 801) = 241400$ clock cycles. This is almost equal to what is achieved with the invention. However, the silicon area costs of this implementation require $200 \times 2 = 400$ bypass flip flops and multiplexers.

Therefore, it can be seen that the invention provides a test access architecture that has the advantages of operating at substantially the same speed as the bypass mode, but

30   without having the additional overhead in terms of bypass hardware.

As mentioned earlier, although the preferred embodiments have been described using an OR gate as the control circuit, it will be appreciated that other forms of control circuit could be used, depending on the status of the control signals.

Furthermore, the OR gate may be located within a test wrapper, within a module itself, or further away in the SOC.

In addition, although the preferred embodiments have been described using two modules, the invention applies to any number of modules connected to the TAM. Also, although the TAM described in the example is two bits wide, the invention is equally applicable to a TAM of any width.

It is also noted that, although the example provided above has been described using one clock cycle for the test launch/capture procedure, it will be appreciated that the launch and capture process may comprise a plurality of clock cycles for certain tests.

It will be appreciated by a person skilled in the art that other variations and modifications are possible, without departing from the scope of the invention as defined by the appended claims.